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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,643	09/05/2000	Pak Shing Chau	RA-194	7634

7590 05/09/2005

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EXAMINER	
BAYARD, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,643	CHAU ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to RCE filed on 2/3/05 in which claims 1-23 are pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Tamura et al U.S. Patent No 6,707,727 B2.

As per claims 1, 12 and 20, Tamura et al teaches a communication system comprising: a first printed circuit board (see figs. 2, 29, 72 and col.1, lines 48-50 and col.38, lines 3-10); a conductive path (see figs. 2, 29, 72 elements 3, 2102, 4020) affixed to the printed circuit board; a driver circuit (see figs. 2, 29, 72 elements 1, 4, 2101, 4010) affixed to the first printed circuit board and coupled to the conductive path to output onto the conductive path a signal having a voltage level that varies time between at least three distinct levels representative of at least three distinct digital values (see col.2, lines 28-65 and col.4, lines 15-18), the driver circuit including an equalization circuit (see fig.72 element 4063 and col.2, lines 65-67 and col.3, lines 28-30 and col.13, lines 19-20 and col.18, lines 5-10 and col.36, lines 5-36) to adjust the voltage level of the signal output by the driver circuit at a first time according to a digital

value represented by the signal at a previous time; and a receiver (see figs. 2, 29, 72 elements 2, 2103, 4060 and col.5, lines 65-67 and col.10, lines 13-14) circuit affixed to the first printed circuit board and coupled to receive the signal from the conductive path to determine which of the at least three distinct digital values is represented by the signal at a given time.

As per claim 2, Tamura et al includes wherein the driver and receiver circuits are respective integrated circuits affixed to the first printed circuit board (see col.38, lines 3-10).

As per claim 3, Tamura et al includes wherein the driver and receiver circuits and conductive path are incorporated within a common integrated circuit that is affixed to the first printed circuit board (see col.38, lines 3-10).

As per claim 4, Tamura et al inherently includes wherein at least one of the driver and receiver circuits is coupled to a second printed circuit board that is affixed to the first printed circuit board.

As per claim 5, Tamura et al inherently includes wherein the second printed circuit board is removably affixed to the first printed circuit board.

As per claim 6, Tamura et al includes wherein the driver circuit receives a plurality of input signals, and the equalization circuit receives and delays said plurality of input signals (see figs.4, 12, 13, 15, 16).

As per claim 7, Tamura et al includes wherein the driver circuit receives a plurality of input signals, and the equalization circuit receives and inverts said plurality of input signals (see figs.4, 12, 13, 15, 16).

As per claim 8, Tamura et al includes wherein the equalization circuit compensates (see col.3, lines 5-6) for attenuation of the signal in the conductive path.

As per claim 9, Tamura et al includes wherein the equalization circuit compensates (see col.3, lines 5-6) for reflection of the signal in the conductive path.

As per claim 10, Tamura et al includes wherein the equalization circuit compensates (see col.3, lines 5-6) for crosstalk generated by the signal in a second conductive path.

As per claim 11, Tamura et al inherently includes wherein said signal has a fourth voltage level that varies in time between at least three distinct levels, the fourth level representative of a fourth digital value that is distinct from the at least three distinct digital values.

As per claim 13, Tamura et al inherently includes wherein for each of said signal levels, an activation level of said main driver and an activation level of said auxiliary driver sum to equal N.

As per claim 14, Tamura et al inherently includes, wherein said equalization mechanism includes an element adapted to invert said input signals.

As per claim 15, Tamura et al inherently includes wherein said equalization mechanism includes an element adapted to delay said input signals by a time substantially equal to a bit period.

As per claim 16, Tamura et al inherently includes wherein said main driver and said auxiliary driver each include a current source, and said signal levels are voltages that are a range between ground and a positive voltage.

As per claim 17, Tamura et al inherently includes wherein said equalization mechanism is configured to compensate for attenuation of said signal over a signal line.

As per claim 18, Tamura et al inherently includes, wherein said equalization mechanism is configured to compensate for reflection of said signal over a signal line.

As per claim 19, Tamura et al inherently includes wherein said signal is transmitted over a first signal line and creates crosstalk in a second signal line, and said equalization mechanism is coupled between said first and second lines and configured to compensate for said crosstalk in said second line.

As per claim 21, Tamura et al inherently includes wherein said main drivers and equalization mechanism each include a current source, and said signal levels are voltages that are in a range between ground and a positive voltage.

As per claim 22, Tamura et al inherently includes, wherein said equalization mechanism further comprises a delay element and a second auxiliary driver having a gain that is substantially proportional to and smaller than said first main driver, said second auxiliary driver configured to receive said first plurality of input signals after delay by said delay element, and to output on said first line a fourth signal.

As per claim 23, Tamura et al inherently includes wherein said equalization mechanism further comprises an inversion element and a second auxiliary driver having a gain that is substantially proportional to and smaller than said first main driver, said second auxiliary driver configured to receive said first plurality of input signals after inversion by said inversion element, and to output on said first line a fourth signal.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimoto et al U.S. patent No 6,414,890 B2 teaches a semiconductor memory device.

Arcoleo et al U.S. Patent No 5,864,506 teaches a memory having selectable output.

Manning U.S. patent No 5,835,440 teaches a memory device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

4/20/05

EMMANUEL BAYARD
PRIMARY EXAMINER